Development of IEEE802.11a WLAN LNA in Silicon-based Processes

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Abstract — **In this paper, we describe the effects of substrate parasitics in silicon-based processes and present a methodology for designing low-noise amplifiers (LNA's) in silicon processes. Our techniques resulted in excellent agreement between simulations and measurements for a test case LNA design for 802.11a. This LNA, which covers 5-6 GHz and has gain switching is designed in a 0.8μm SiGe bipolar technology with f_T of 50 GHz. The LNA exhibits a gain of more than 24dB in the 5-6 GHz band with a Noise Figure (NF) less than 2.5dB. The agreement between simulation and measured data is demonstrated.**

I. MOTIVATION

With the ever-increasing frequencies of operation of wireless communication systems, it becomes more and more challenging to design RF front-end circuits in silicon substrates. The real challenge in silicon-based processes such as Si-CMOS or SiGe HBT is the substrate coupling effects that become increasingly significant to the performance of the circuit at high frequencies [1]. The lossy nature of the substrate makes it even more difficult to achieve desired performance. The motivation behind this work is to develop a methodology for design of high frequency circuits in silicon. This methodology will help to streamline the design of high frequency ICs in Silicon and facilitate the integration of RF and baseband circuits.

In this work, we present a 5-6 GHz Low-Noise Amplifier (LNA) designed in a 0.8μm SiGe bipolar technology for IEEE802.11a applications. A great deal of attention was given to the substrate modeling and its impact on feedback within the amplifier. The losses through the substrate were also modeled in simulation and showed very good agreement with the measurement results.

II. SUBSTRATE EFFECTS IN SILICON

Coupling through the silicon substrate is a significant problem in designing Silicon RF ICs. This is due to the non-ideal isolation provided by the common substrate shared between different circuits components on the chip.

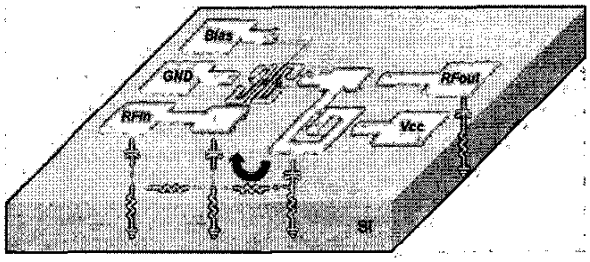

Fig.1. The effects of substrate parasitics in silicon. A positive feedback from an inductor to a capacitor is shown as an example.

The interaction through the substrate is present also between different devices of the same circuit. This needs to be taken into account during the design [1]-[2]. Fig. 1 shows an example of the typical substrate parasitic effect that exists in silicon. Generally, the parasitics affect the performance of the LNA by lowering the gain and increasing the noise figure. This is due to undesirable feedback and shift in the input and output match. Also, appreciable positive feedback can lead to oscillations in the circuit.

Fig.2 shows a typical example of how the parasitics were modeled in simulations. A feedback path consisting of a capacitor in series with a resistor is placed between the collector and the base of a transistor to account for the substrate coupling.

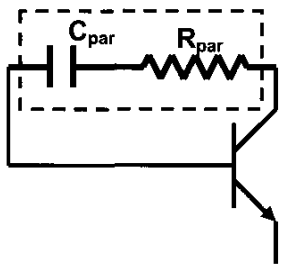

Fig. 2. Illustration of how the substrate modeling was introduced in simulations.

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The value of the resistance and the capacitor (R_{par} and C_{par}) depends on the distance between the points, resistivity of the substrate and the thickness of the dielectric layer between the metal line and the substrate. In our case, the resitivity of the material was 20-Ω-cm. The substrate resistances were of the order of few hundreds (300-400) of ohms for a distance of about 200 μm. Also, the feedback capacitors were of the order of 0.01-0.05pF. The capacitance was calculated using the standard formula:

$$C = (\varepsilon_0 \varepsilon_r L/A) \quad (1)$$

The metal lines used in the layout for connection has also been modeled as a distributed transmission line, as shown in Fig. 3 below. R_{Line} is estimated using the given resistivity of the metal, while C_{Line} takes into account the dielectric constant of the material and the thickness of the dielectric layer between the metal line and the substrate. R_{sub} is estimated to be a constant resistance for a metal layer (which in our case was approximately 500Ω). The inductor (L_{Line}) is estimated from the substrate parameters as in case of a microstrip line [4]. In many cases, like inductors, the distance between the two ends are appreciably large so the estimation of the parasitics was done for the two ends separately and an average was taken. The equivalent model for this case is shown in Fig. 4 where the feedback is distributed between the two ends.

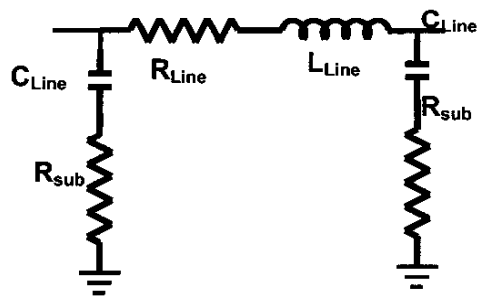


Fig. 3. Transmission line model used for the metal connectors in the layout.

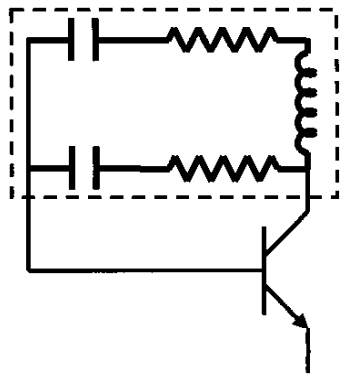


Fig. 4. Typical model for the distributed feedback in case of a large component like inductor.

III. 5-6 GHZ SIGE LNA

The 5-6GHz LNA was designed in a 0.8μm SiGe process with f_T of 50GHz. The simplified schematic of the LNA is shown in Fig.5. The LNA is a 3-stage common emitter design. The second-stage of the LNA is used for gain switching, while the first and third stages are used as a buffer to keep the input and output impedances matched to 50-ohm between high and low-gain modes. The two-modes of operation, high-gain and low-gain are to account for the large signal magnitude in case of close proximity of the receiver with the source. In this case, the gain is reduced so as to limit the signal power so that it does not saturate the circuit blocks which follow the LNA in the complete receiver.

Fig. 6 shows the schematic of the LNA with the effect of parasitics taken into account while designing. The modeled parasitics are plugged into the simulations and the circuit is further optimized. The metal line models are not shown in this figure but included during simulations.

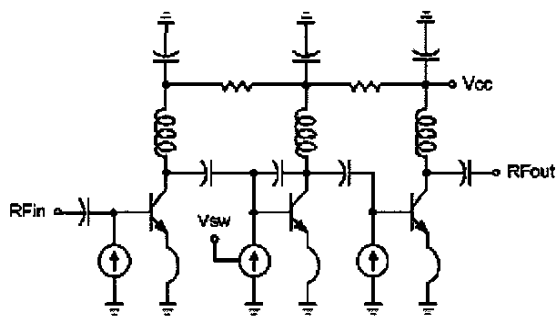


Fig.5. Simplified circuit schematic of the Switched-Gain LNA.

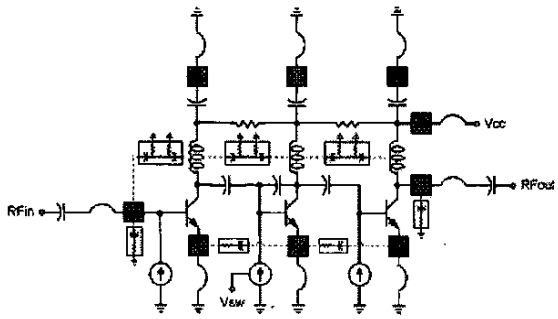
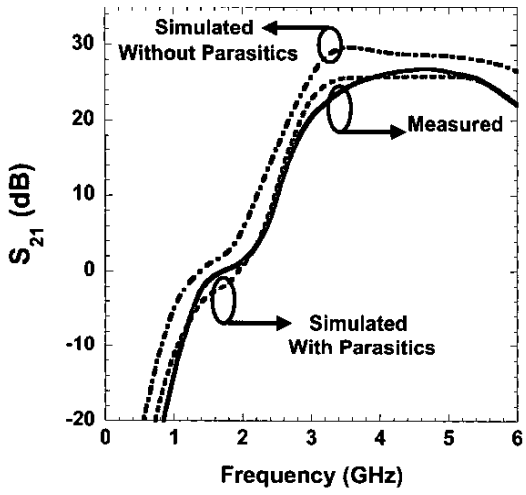
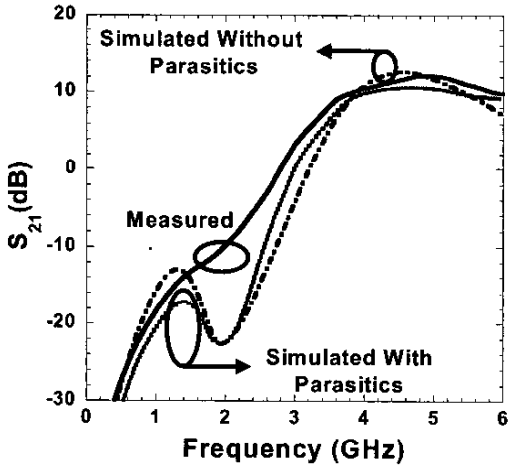


Fig.6. Circuit schematic of the LNA with substrate effects.

Fig. 7 shows the correspondence between simulations and measured results of the LNA in high and low gain modes.



(a)



(b)

Fig.7. Simulated and measured S_{21} of the 5-GHz LNA for (a) High-Gain Mode, and (b) Low-Gain Mode.

Fig.8. shows the measured gain and noise figure of the LNA in both the high and low-gain modes. As shown, this topology yields not only a low noise figure of 2.5dB in the high-gain mode, but also maintains a noise figure below 4dB in low-gain mode over the entire 5-6 GHz band.

Table 1 shows the complete measured performance of the LNA. The supply voltage used for the LNA is 3V. The IIP_3 measurement was performed with two tones at 5.5GHz and 5.499 GHz.

Clearly, the performance of this LNA is comparable or better than the other works reported in SiGe at this frequency [5]-[6]. The linearity requirements for 802.11a can be efficiently met with the performance of this LNA.

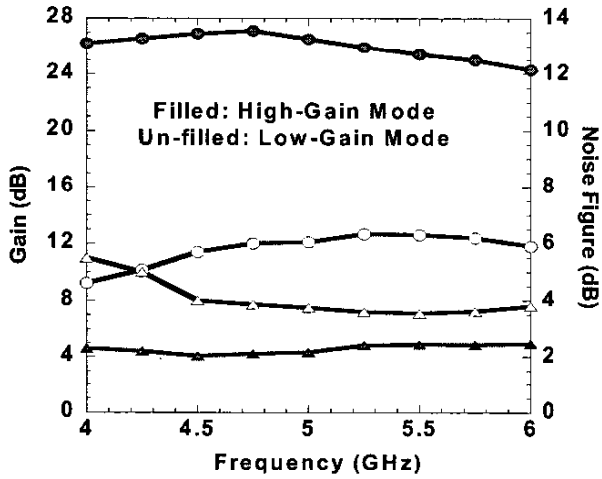


Fig.8. Measurement results of 5-GHz LNA in High-Gain and Low-Gain Modes of operation.

	High-Gain Mode	Low-Gain Mode
Gain	25 dB	12 dB
Noise Figure	2.5 dB	3.7 dB
IIP_3	-13 dBm	-2.3 dBm
Input Return Loss	12 dB	8 dB
Current Drawn	18 mA	16 mA
Power Consumption	54 mW	48 mW

Table 1. Measured data for the 5-GHz LNA at 5.5 GHz. Supply voltage used is 3V.

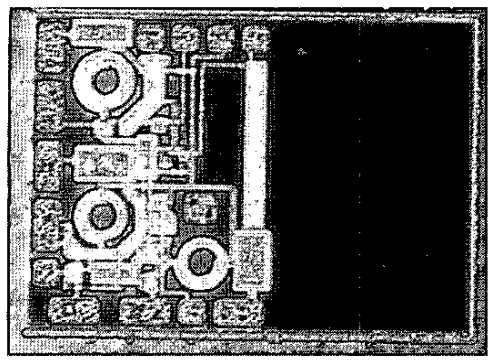


Fig.9. Die Photograph of the LNA.

Fig. 9 above, shows the die-photograph of the LNA. The die-size is 620μm x 790μm. The bonding diagram of the LNA is shown in Fig. 10.

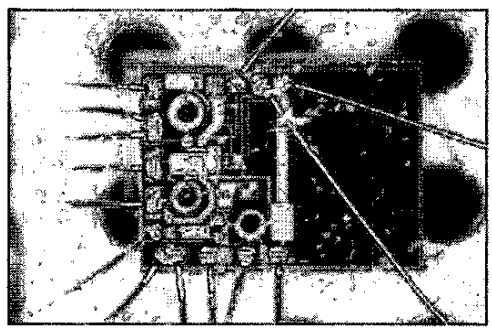


Fig. 10. Bonding diagram of the LNA.

V. CONCLUSION

In this paper we demonstrated a methodology for design of high frequency silicon LNAs. This methodology allows for accurate simulation of key performance criteria and accounts for impact of substrate. Measurement show excellent correlation with the simulation results verifying our techniques. The parasitic effects of the silicon substrate are taken into account during the design and a good agreement has been established between simulated and measured data. A measured gain of more than 24dB is achieved in the 5-6 GHz band. The noise figure was seen to be better than 2.5dB in the same band.

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